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Applicant : HEIKO HOMMEN ET AL.

Filed : CONCURRENTLY HEREWITH

Title : METHOD FOR EXPOSING AT LEAST ONE OR AT LEAST TWO SEMICONDUCTOR WAFERS

CLAIM FOR PRIORITY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Claim is hereby made for a right of priority under Title 35, U.S. Code, Section 119, based upon the European Patent Application 01 104 358.5, filed February 23, 2001.

A certified copy of the above-mentioned foreign patent application is being submitted herewith.

Respectfully submitted,

For Applicants

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Bescheinigung

Certificate

Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

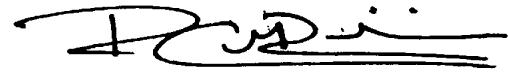
Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. Patent application No. Demande de brevet n°

01104358.5

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office
Le Président de l'Office européen des brevets
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R C van Dijk

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**Blatt 2 der Bescheinigung
Sh et 2 of the certificate
Page 2 de l'attestation**

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Application no.: 01104358.5
Demande n°:

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Applicant(s):
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Method for exposing at least one or at least two semiconductor wafers

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Etats contractants désignés lors du dépôt:

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Remarks:
Remarques: The application was transferred from the original applicant Semiconductor300 GmbH & Co. KG, Dresden, Germany, to the above-mentioned applicant on 19.02.02.

23 Feb. 2001

Description

Method for exposing at least one or at least two semiconductor wafers

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The present invention relates to a method for exposing at least two semiconductor wafers with a pattern, the exposure being performed in an exposure tool, an alignment being performed in response to a first set of alignment parameters, 10 which depends on characteristics of each of said wafers, and a second set of alignment parameters, which accounts for an exposure tool-offset, and to a method for exposing at least one semiconductor wafer.

15 In semiconductor wafer manufacturing the tool and process control is one of the main issues for providing high quality and efficiency of the device output of a manufacturing facility. Typically, process control is performed by measuring some characteristics of a group of wafers, e.g. a lot, after 20 the wafers have been processed in a manufacturing tool. One example is measuring a critical dimension of semiconductor wafers in a lot after exposure. The lot is usually processed in a batch. Since processing tools and inspection tools are commonly grouped in different parts of a fab, wafers combined 25 in a lot travel through the fab after the batch is finished with processing. Eventually, the wafers of the lot are measured in an inspection tool and the measured characteristics may reveal problems with the processing tool, such as focus, alignment, coating or development problems in the case of wafers being processed in a lithographic cluster. These problems can often be fixed by adjusting tool parameters, which 30 are used to process wafers. Accordingly, having adjusted the processing tool setup using the inspection results as an input for correcting tool parameters, the next incoming batch 35 or lot of semiconductor wafers can be processed with improved sets of tool parameters, resulting in an increased production yield.

Usually these measurements in an inspection tool are based on dynamic or static sampling. Typically, not every device in a batch is controlled, rather statistical methods are used to 5 pick out a subsample of the lot for the measurement and the results are feeded back for the new incoming batch devices, which are to be processed. Thereby, it is assumed that the next incoming batch devices being manufactured with improved tool parameters behave in the same manner as the previous 10 batch with respect to the tool parameters, which might not always be the case.

Using this conventional method of statistical process control (SPC) several further disadvantages arise. One is that processed wafers of a batch or lot, that have selectively just 15 been measured in an inspection tool indicating problems with the process tool setup, all have to be moved into rework because they are each most probably affected by these problems. Therefore, free inspection tool capacity as well as the 20 throughput and yield of the process tool are disadvantageously reduced.

Furthermore, problems with single devices might not be covered, if, e.g., always just a first wafer in a lot is affected by a problem but it is not selected for inspection by 25 statistical sampling. In this case the origin of a parameter drift in a process tool might not be recognized, or tool parameters might be adjusted inappropriately in reaction to a measured parameter drift. Thus, expensive process tool capacity is wasted and the time to manufacture a device is disadvantageously increased.

It is therefore a primary objective of the present invention to accelerate the throughput of lots or batches of semiconductor wafers in a process tool, to increase the wafer yield 35 and to save costs in semiconductor wafer manufacturing.

The objective is solved by a method for exposing at least two semiconductor wafers with a pattern, the exposure being performed in an exposure tool, an alignment being performed in response to a first set of alignment parameters, which depend

5 on characteristics of each of said wafers, and a second set of alignment parameters, which account for an exposure tool-offset, comprising the steps of providing a first semiconductor wafer to said exposure tool for exposing said wafer, performing alignment of said first semiconductor wafer, with determining values for said first set of alignment parameters, exposing the first semiconductor wafer using the combination of said first and second sets of alignment parameters, determining values for a set of parameters representing the overlay accuracy of said first pattern on said first semiconductor wafer, adjusting values of said second set of alignment parameters to correct for an overlay inaccuracy of said pattern, exposing a semiconductor wafer including an alignment in response to said adjusted values.

20 Using the method according to the present invention the overlay measurement results of a first semiconductor wafer, which can be determined in several ways, are used to change the tool parameter setup for the following or any other second wafer in a batch. In the context of this invention the alignment is performed using two sets of alignment parameters. The first set of alignment parameters describes the way, in which an individual wafer is aligned and how the grid of exposure fields is set on the wafer. Examples of such parameters are the chip magnification, shifts in x- and y-direction, grid

25 scaling in x- and y-direction, orthogonality of x- and y-direction, chip rotation, etc. These parameters are used for wafer steppers and scanners, whereby in the case of scanners the chip magnification is adjustable in x- and y-direction separately. Such parameters are determined during an alignment prior to any exposure of a wafer.

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The same parameters but with different values build up the second set of alignment parameters, which accounts for the exposure tool-offset. These offset values are each added to or subtracted from the corresponding parameters of the first 5 set of alignment parameters after the values of said first set have been determined. These tool-offset parameters are used to correct for misalignments during the alignment of the semiconductor wafer.

10 Having determined the values for a set of alignment parameters representing the overlay accuracy of the pattern on the first semiconductor wafer, that just has been exposed or is to be exposed in the exposure tool, the quality of the alignment performance can be checked. Generally, sets of parameters 15 representing the overlay accuracy can be related to sets of alignment parameters. Therefore, according to the present invention the second set of tool-offset alignment parameters is adjusted in its values to correct for an overlay inaccuracy of the pattern that either has been exposed or is to be 20 exposed in case that the overlay data reveal values beyond a tolerance level.

The objective can further be solved using a similar method, where the tool-offset parameters can be adjusted using already 25 at least one semiconductor wafer. With each further wafer that is aligned and optionally exposed, the tool-offset parameters can even be further refined. The corrected tool-offset parameters necessarily will lead directly to an improved tool-setup, due to which the yield is advantageously 30 increased. Moreover, the method according to the present invention may be combined with a method similar to the advanced process control in the sense that the present method may be repeated a few times until there repeatedly is no adjustment 35 of the values of the second set of alignment parameters necessary, after which the determination step for the values of the set of parameters representing the overlay accuracy can be skipped. Thus, the application of the method of the pres-

ent invention leads to a situation, where costs can be saved due to a reduced amount of inspection time for wafers after exposure. Furthermore, the increased yield advantageously leads to a decreased throughput time.

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In a another aspect of the present invention the case of calculating the parameters reflecting the overlay accuracy using a formula and adjusting the second set of alignment parameters, i.e. the tool-offset alignment parameters, is each performed prior to exposing the semiconductor wafer. This aspect of the method according to the present invention has the advantage, that the wafer is not exposed, until the sets of alignment parameters are arranged with values, that provide sufficient quality for the eventual exposure. Therefore, the yield is still further increased, the throughput time even further decreased and the costs are advantageously reduced.

In a further aspect the step of determining the values for the set of parameters representing the overlay accuracy is considered to be performed by calculating the values from those alignment parameters, that have been determined in the exposure tool alignment, i.e. the first set of alignment parameters. This calculation can be based on the fact, that an overlay parameter measured with an inspection tool can as well be derived or calculated with a mathematical formula comprising a combination of alignment parameters of the first set, each of them being supplied with a coefficient, which depends on the exposure tool. This determination is found to recover a sample of measurements of corresponding overlay parameters to a high degree of accuracy. The coefficients have to be determined once for a complete tool-offset and can then be reused until the next complete setup of the corresponding exposure tool is performed. Typically, this is a duration of weeks or months.

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Therefore, the overlay parameters are known immediately after the alignment in the exposure tool when the determination of

the corresponding alignment parameters is finished. This preferentially happens by means of an alignment measurement. Since the values for the set of overlay parameters are known from the calculation, a measurement with an inspection tool

5 can be skipped resulting in a further reduced wafer throughput time. The second set of alignment parameters, i.e. the tool-offset alignment parameters are then adjusted according to the set of calculated overlay parameters.

10 In a further aspect the mathematical formular for calculating the values of the set of parameters representing the overlay accuracy is considered to be a linear function with the coefficient in front of each alignment parameter being dependent on the exposure tool employed. A high degree of accuracy for

15 recovering the overlay measurement results with a linear function is found, resulting in an easy and straightforward calculation step. Only a few coefficients are involved in this case.

20 In a further aspect the stopping of the batch queue as a result of values for the set of the parameters representing the overlay accuracy exceeding threshold values corresponding to tolerance levels is considered. After the batch or lot processing is stopped system maintenance can be conducted in re-

25 sponse to a warning signal, that has been issued in this case. After having reset said exposure tool processing of semiconductor wafers can be continued.

30 In a further aspect a second determination of the values of the set of parameters representing the overlay accuracy of the wafer pattern is considered. A warning signal is issued, when one of the parameters of the set of parameters representing the overlay accuracy of the pattern increases beyond a pre-determined tolerance level. A detailed investigation of

35 the parameters and the reason why the tolerance level has been exceeded, can than be performed by remeasuring values of the overlay parameters, which priorily have been calculated

using the formular from the first set of alignment parameters.

5 In a further aspect it is considered that each of the at least two semiconductor wafers is processed in a next manufacturing step after exposure without being inspected in an overlay tool.

10 In a further aspect it is considered, that also the values for the set of tool-offset alignment parameters are calculated from the set of parameters representing the overlay accuracy using a linear formula. This feature provides a fast feedback for the alignment procedure from the overlay parameter determination.

15 In a furhter aspect, a neuronal network is built by means of the results of the calculation of the values for the set of parameters representing the overlay accuracy performed by a control unit 100 in comparison with the measurement of the 20 values for the set of parameters representing the overlay accuracy in the inspection tool 40, for adjusting the formula for calculating said values for the set of parameters representing the overlay accuracy.

25 The invention will be better understood by reference to the following description of embodiments of the invention taken in conjunction with the accompanying drawings, wherein

30 figure 1 schematically shows the wafer process flow in lithography as well as the alignment feedback according to an embodiment of the present invention,

35 figure 2 displays the same as in figure 1, but for an embodiment comprising an offset adjustment prior to exposure according to the present invention,

figure 3 displays a diagram of grid scale data in x- and y-direction measured as a wafer alignment parameter during an alignment for the exposure of DRAM wafers within a period of 3 months versus exposure date,

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figure 4 shows a diagram with used values for the tool-offset parameter chip magnification according to prior art (diamonds) versus date, overplotted with calculated offset values (squares) for the same parameter according to an embodiment of the present invention, for the exposure of the same DRAM wafers as displayed in figure 3,

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figure 5 shows a plot of the overlay parameter chip magnification representing the overlay accuracy of a pattern as measured with an KLA overlay inspection tool, with and without applied tool-offset (diamonds and circles, resp.) according to prior art, and as being calculated (squares) according to an embodiment of the present invention, for the same DRAM wafers as displayed in figure 3, versus date.

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The control of the wafer flow through processing steps 20, 30, 40, 90 according to an embodiment of the method of the present invention is shown in figure 1. There, thick arrows denote the physical wafer flow, while narrow arrows denote a flow of information, either signal and/or the data corresponding to the sets of alignment parameters. A semiconductor wafer batch queue 10 is provided for exposure. Prior to being exposed in an exposure step 30 a first semiconductor wafer 1 of the batch undergoes an alignment step 20 on the wafer stage inside the exposure tool 35.

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After the wafer has been exposed the wafer alignment parameter data, which are measured during the alignment step 20, are examined in a control unit 100. Thereby, using the wafer alignment parameter data it calculates the relevant inspec-

tion overlay data, i.e. values for the set of overlay parameters representing the overlay accuracy of the pattern that is structured on the first semiconductor wafer 1.

5 For example, the chip magnification expressed as an overlay parameter is calculated using a linear formula

```
chip_mag(overlay) =  
1.24 + 0.50 · scale_x + 0.50 · scale_y + chip_mag(align)
```

10 where `chip_mag(overlay)` denotes the chip magnification as a parameter representing the overlay accuracy, `chip_mag(align)` denotes the chip magnification as a wafer alignment parameter as determined during the alignment step, `scale_x` and `scale_y` denote the grid scaling in x- and y-direction, respectively.

15 The coefficients 1.24, 0.50 and 0.50 are exposure tool-dependent and are fixed for the duration of a typical tool setup.

20 The calculated overlay parameter values are then compared each with parameter dependent tolerance levels according to the overlay accuracy specification provided for the product. If one the one side the calculated overlay data provide sufficient results, i.e. within a tolerance range, the wafer is forwarded to the next process step 90. On the other side if 25 the overlay data reveal calculated values that increase beyond said tolerance levels, the wafer is forwarded to an inspection tool 40 for performing a second determination of the overlay parameters, i.e. a measurement. If this measurement actually reveals insufficient overlay quality the wafer is 30 sent into rework 50, while it can be forwarded to the next process step 90 in case the overlay measurement reveals oppositely sufficient overlay accuracy. In the latter case a re-determination of the calculation formula used in control unit 100 for determining the values for the set of overlay parameters from the values of the set of wafer alignment parameters 35 might be appropriate. Nevertheless, the new alignment offset

can be determined by control unit 100 according to measurement results of the inspection tool 40 as described below.

While a warning signal 105 is issued by the control unit 100 for controlling the further processing of the semiconductor wafer 1 as described above, also adjusted values for the set of tool-offset parameters are determined by control unit 100 for the alignment procedure. These values are to be added to the values of the set of wafer alignment parameters that are determined during the alignment step 20. A second semiconductor wafer 2 is then aligned and exposed in the exposure tool 35 using the adjusted tool-offset parameter values as indicated by the dashed line in the exposure unit 30 of figure 1, that correct for a possible misalignment derived by control unit 100 for the first semiconductor wafer 1. The alignment data may also be received by the control unit 100 prior to exposure, but the feedback to the alignment step 20 is only provided for the alignment of the following second semiconductor wafer 2. The exposure of the first semiconductor 1 is performed using the originally given values for the set of tool-offset alignment parameters (the first set of alignment parameters).

Another embodiment of the present invention is shown in figure 2. It deviates from the embodiment shown in figure 1 by a closed loop feedback from control unit 100, which performs the wafer alignment parameter determination, the overlay parameter calculation and the tool-offset parameter adjustment already after the alignment 20 prior to wafer being exposed in exposure step 30. Semiconductor wafer 1 is aligned, while values for the alignment parameters are received by control unit 100. As in the previous embodiment control unit 100 then calculates values for the set of overlay parameters representing the overlay accuracy. Because the semiconductor wafer 1 is not yet exposed and still performing the alignment step 20, the tool-offset alignment parameters can be adjusted in-situ in case the overlay accuracy - and thus the tool-offset

- can still be improved for the same first semiconductor wafer 1.

5 After being exposed an overlay control can optionally be issued by means of statistical process control (SPC) 101 for performing a statistical verification of the overlay results calculated due to the control unit 100.

10 A comparison of the method according to the present invention with prior art is indicated in figures 3 - 5. As an example the tool-offset parameter for chip magnification is derived using wafer alignment parameters like grid scale in x- and y-direction as input for the calculation. The grid scaling in both directions for a measurement period of several wafers 15 during a period 3 months is shown in figure 3. There, it can easily be seen, that e.g. the grid scaling in y-direction is scattering around each of the two distinct values of about 1.3 and 3 ppm.

20 It has been found, that the altering grid scaling expressed as an alignment parameter has an influence on the chip magnification expressed as a parameter representing the overlay accuracy. Therefore, the chip magnification - this time expressed as an alignment parameter - can be provided with an 25 offset to correct for the jumps in the grid scaling data.

In figure 4 the corresponding tool-offsets, that have been used to provide a conventionally optimum overlay accuracy, are displayed as diamonds. They were fixed at five distinct 30 values for the tool-offset alignment parameter chip magnification, which were: initially 1.3 ppm, then 2 ppm, followed by 1 ppm, followed by 3 ppm and finally 1.9 ppm during the same period of 3 months, and for the same exposure tool and wafers as in figure 3.

35 In figure 5 the corresponding diamonds reveal the final outcome for the overlay accuracy with respect to chip magnification. This prior art case is characterized by a large scatter

between +2 ppm and -2 ppm in chip magnification. The distinctly set tool-offset parameter chip magnification (diamonds in figure 4) provided a linear shift (offset) in figure 5 from the data represented by the circles, which represent

5 the measured chip magnification overlay parameter as being measured without an offset applied during the alignment.

Thus, the distinctly set offset parameters shifted the measured overlay data advantageously into the tolerance window for overlay, which, e.g., may be represented by a range for

10 chip magnification between -1 ppm and +1 ppm. But this handset chip magnification offset cannot impede the large scatter that is obvious from figure 5 from the diamonds as well as the circles. In this prior art case, the amount of rework therefore is disadvantageously large.

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Using the embodiment of the present invention, e.g. according to figure 2, the tool-offset parameter chip magnification may be calculated individually for each wafer. A linear formula is used, given by

20 $\text{chip_mag}(\text{offset}) = 4.21 - 0.44 \cdot \text{scale_x} - 0.55 \cdot \text{scale_y}$,
whereby $\text{chip_mag}(\text{offset})$ denotes the tool-offset parameter chip magnification, and scale_x and scale_y denote the wafer alignment parameter grid scaling in x- and y-direction, respectively. The coefficients 4.21, 0.44 and 0.55 have been

25 determined previously in the context of a change of the tool setup, e.g. after a maintenance.

The ideal offset calculated using this formula is displayed as a set of squares in figure 4. The data scatter around the

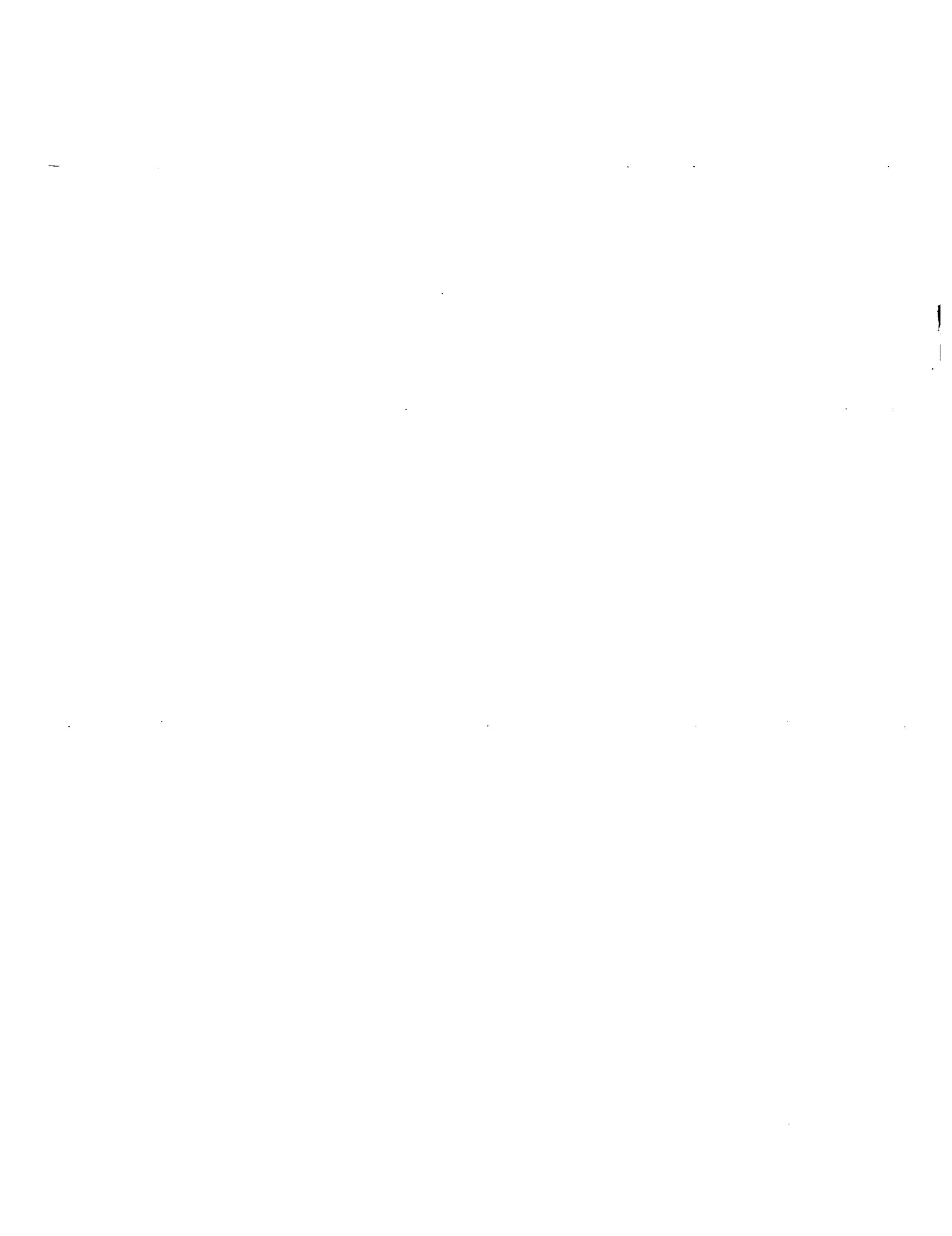
30 conventionally derived tool-offset chip magnification. But

because this scatter originates from a correction of the scatter in the chip magnification overlay data, the quality

of the overlay results has strongly increased as can be seen by the squares in figure 5. All values for the overlay chip

35 magnification are within the tolerance level of -1 ppm to +1 ppm. Thus, the yield is advantageously increased and the throughput time efficiently reduced. Moreover, free inspec-

tion tool capacity is gained, since the overlay control in most cases can be skipped using the method according to the present invention.



Claims:

1. Method for exposing at least two semiconductor wafers (1, 2) with a pattern, the exposure being performed in an exposure tool (35), an alignment (20) being performed in response to a first set of alignment parameters, which depends on characteristics of each of said wafers (1, 2), and a second set of alignment parameters, which accounts for an exposure tool-offset, comprising the steps of:
 - 10 i) providing a first semiconductor wafer (1) to said exposure tool (35) for exposing said wafer,
 - ii) performing an alignment (20) of said first semiconductor wafer (1), with determining values for said first set of alignment parameters,
 - 15 iii) exposing the first semiconductor wafer using a combination of said first and second sets of alignment parameters,
 - iv) calculating the values for a set of parameters representing the overlay accuracy of said first pattern on said first semiconductor wafer (1) from said first set of alignment parameters,
 - v) adjusting values of said second set of alignment parameters to correct for an overlay inaccuracy of said pattern,
 - 25 vi) exposing said second semiconductor wafer (2) including an alignment (20) in response to said adjusted values.
2. Method for exposing at least one semiconductor wafer (1) with a pattern, the exposure being performed in an exposure tool (35), an alignment being performed in response to a first set of alignment parameters, which depends on characteristics of each of said wafers, and a second set of alignment parameters, which accounts for an exposure tool-offset, comprising the steps of:
 - 35 i) providing said at least one semiconductor wafer (1) to said exposure tool (35) for exposing said wafer,

- ii) performing an alignment (20) of said at least one semiconductor wafer, with determining values for said first set of alignment parameters,
- 5 iii) calculating values for a set of parameters representing the overlay accuracy of said pattern on said at least one semiconductor wafer (1) from said first set of alignment parameters,
- iv) adjusting values of said second set of alignment parameters to correct for an overlay inaccuracy of said pattern,
- 10 v) exposing said at least one semiconductor wafer (1) including an alignment (20) in response to said adjustment using a combination of said first and second sets of alignment parameters for the wafer alignment.

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3. Method according to claims 1 or 2, characterized in that a formula is used to calculate said values of said set of parameters representing the overlay accuracy, which is a linear function with coefficients for each alignment parameter.

4. Method according to anyone of claims 1, 2 or 3, characterized by

- issuing a warning signal (105), when one of the parameters of said set of parameters representing the overlay accuracy of said pattern increases beyond a predetermined tolerance level,
- stopping the processing with said exposure tool (35) for conducting system maintenance in response to said warning signal (105),
- 25 - continuing with processing after resetting said exposure tool (35).

30 35 5. Method according to anyone of claims 1, 2 or 3, characterized by

- issuing a warning signal (105), when one of the parameters of said set of parameters representing the overlay accuracy

of said pattern increases beyond a predetermined tolerance level,

- said set of parameters reflecting the overlay accuracy of said pattern on said semiconductor wafer is derived for a second time by measuring the parameters with an overlay inspection tool (40) after the semiconductor wafer (1) has been exposed with said pattern.

6. Method according to anyone of claims 1 to 5,
10 characterized in that each semiconductor wafer is processed in a next manufacturing step after exposure (30) without being inspected in an overlay inspection tool (40).

15 7. Method according to anyone of claims 1 to 6,
characterized in that the adjustment step for the values of said second set of alignment parameters is performed by calculating the values of said second set of alignment parameters from the values of
20 said set of parameters representing the overlay accuracy using a formula, which is a linear function with coefficients for each alignment parameter.

25 8. Method according to anyone of claims 3 to 7,
characterized in that a neuronal network is built by means of the results of the calculation of the values for the set of parameters representing the overlay accuracy performed by a control unit (100) in comparison with the measurement of the values for
30 the set of parameters representing the overlay accuracy in the inspection tool (40), for adjusting the formula for calculating said values for the set of parameters representing the overlay accuracy.

Abstract

23. Feb. 2001

Method for aligning and exposing at least one or at least two semiconductor wafers

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Semiconductor wafers (1, 2), e.g. a lot (10), are exposed after an alignment (20) in a wafer stepper or scanner (35) with each determining their alignment parameters. Using, e.g., a linear formula with tool specific coefficients the overlay accuracy can be calculated from these alignment parameters in advance to a high degree of accuracy as if a measurement with an overlay inspection tool (40) had been performed. The exposure tool-offset can be adjusted on a wafer-to-wafer basis to correct for the overlay inaccuracy derived. Moreover, the alignment parameters for a specific wafer can be used to change the tool-offset for the same wafer prior to exposure. The required inspection tool (40) capacity is advantageously reduced, the wafer rework decreases and time is saved to perform the exposure step (30).

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Figure 1

List of reference numerals:

- 1 first semiconductor wafer
- 2 second semiconductor wafer
- 5 10 batch or lot of wafers
- 20 alignment
- 30 exposure step
- 35 exposure tool
- 40 overlay inspection
- 10 50 rework
- 90 next process step
- 100 control unit
- 101 statistical process control
- 105 warning signal

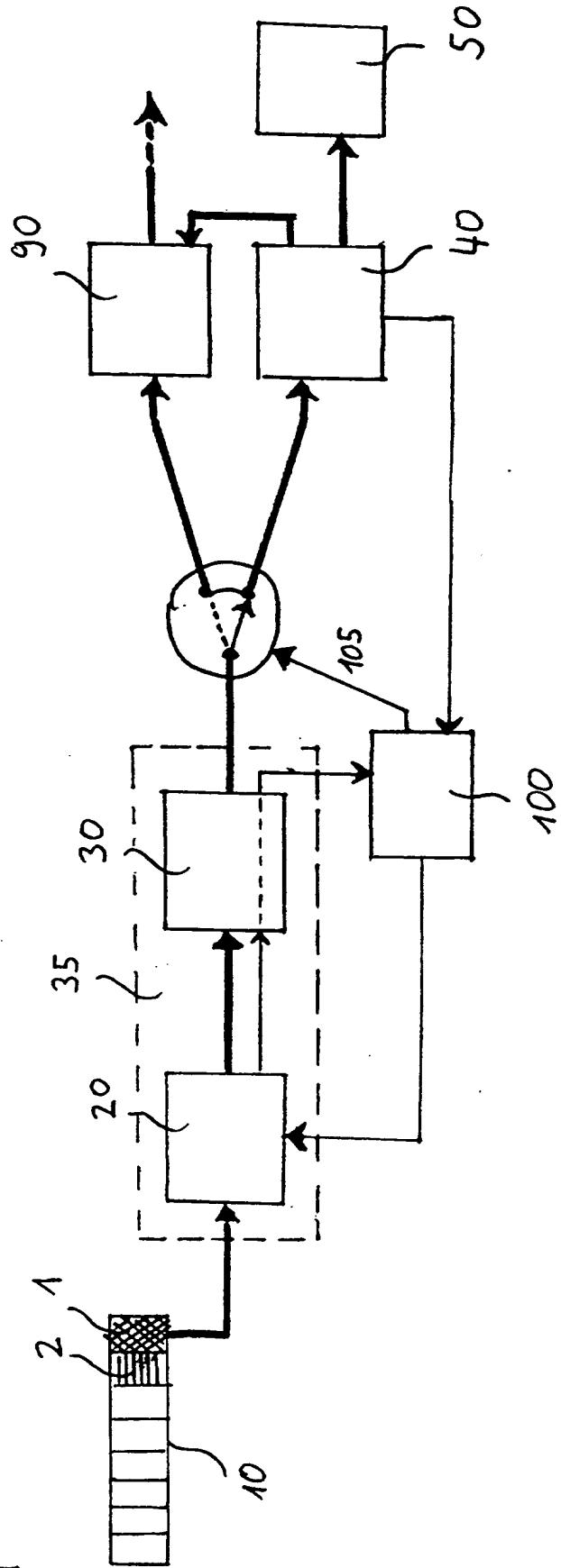


Fig. 1

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23. Feb. 2001

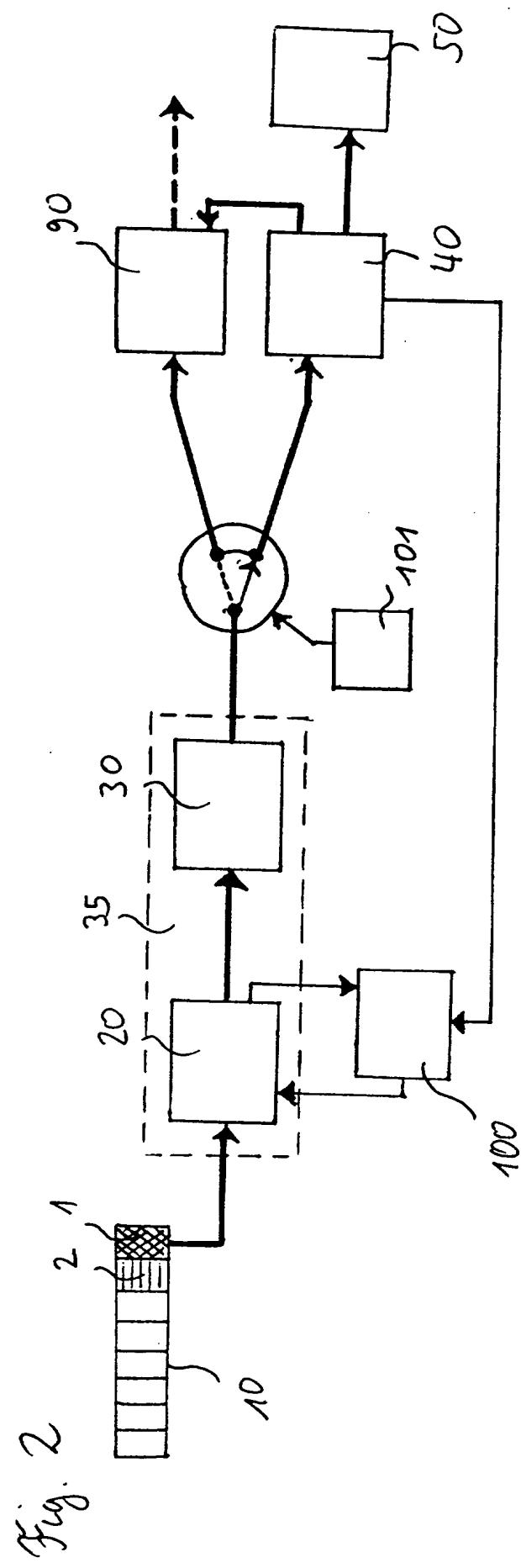


Fig. 3

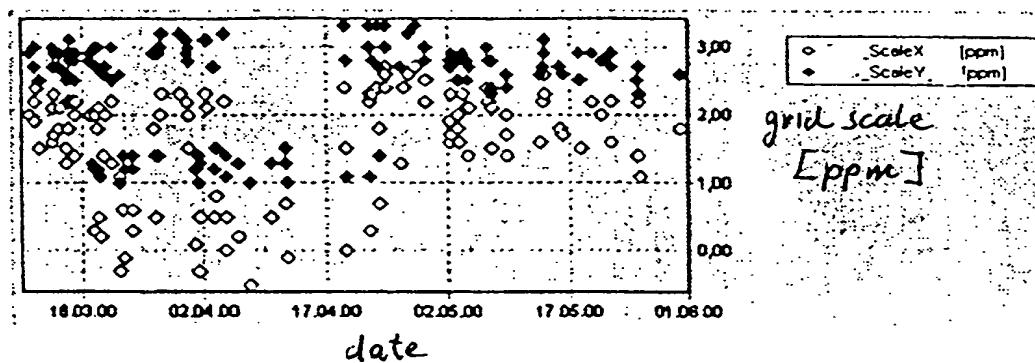


Fig. 4

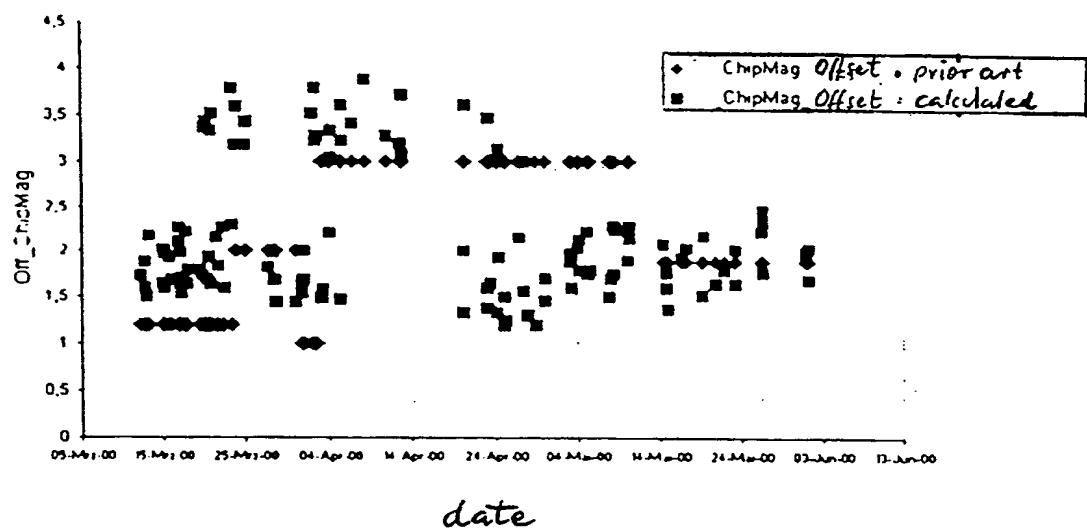


Fig. 5

